

FIG. 1(b)

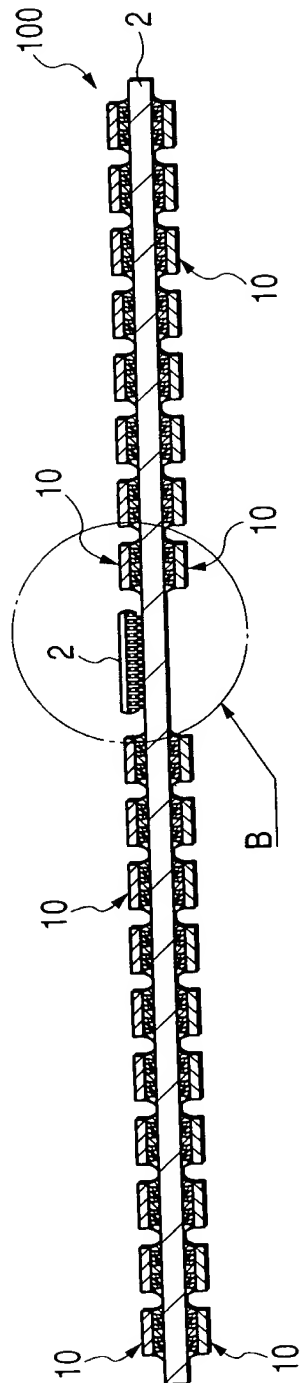


FIG. 1(c)

FIG. 3

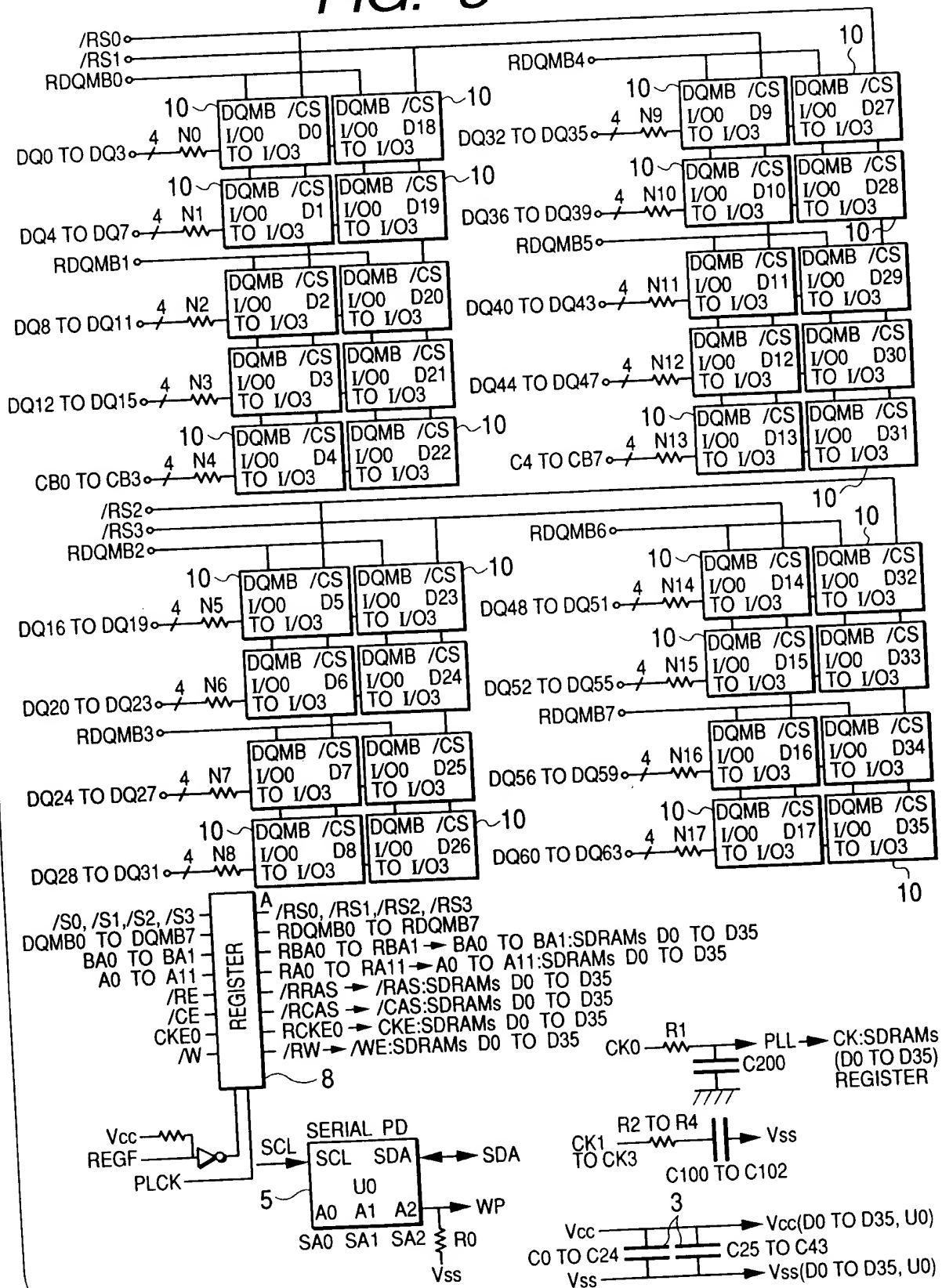


FIG. 4

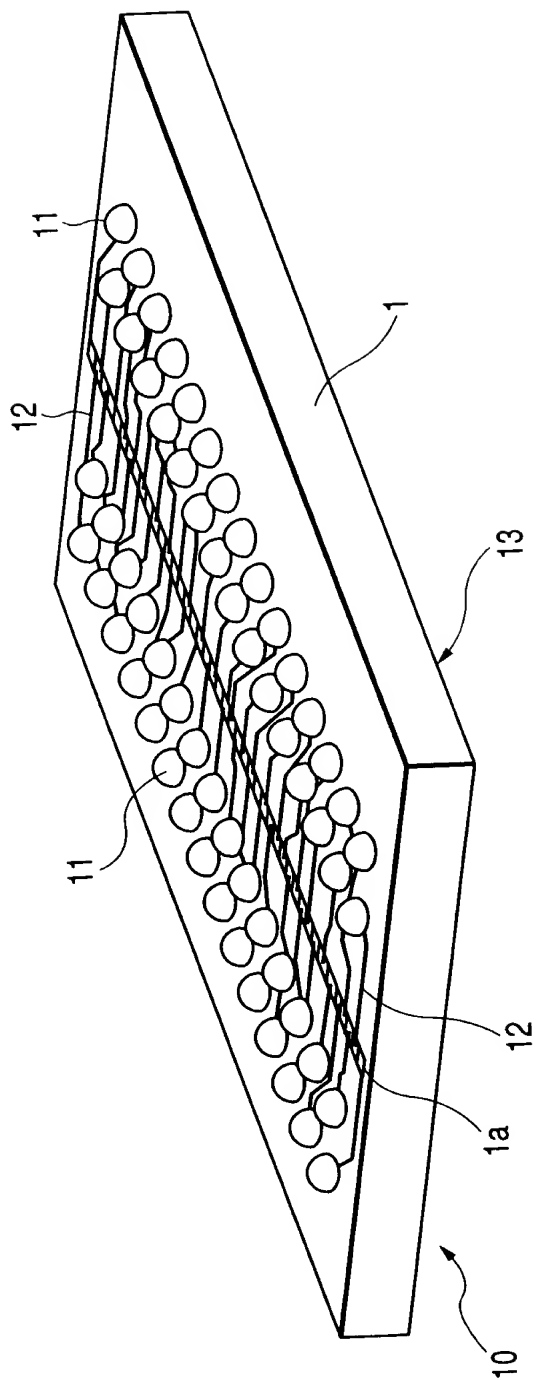
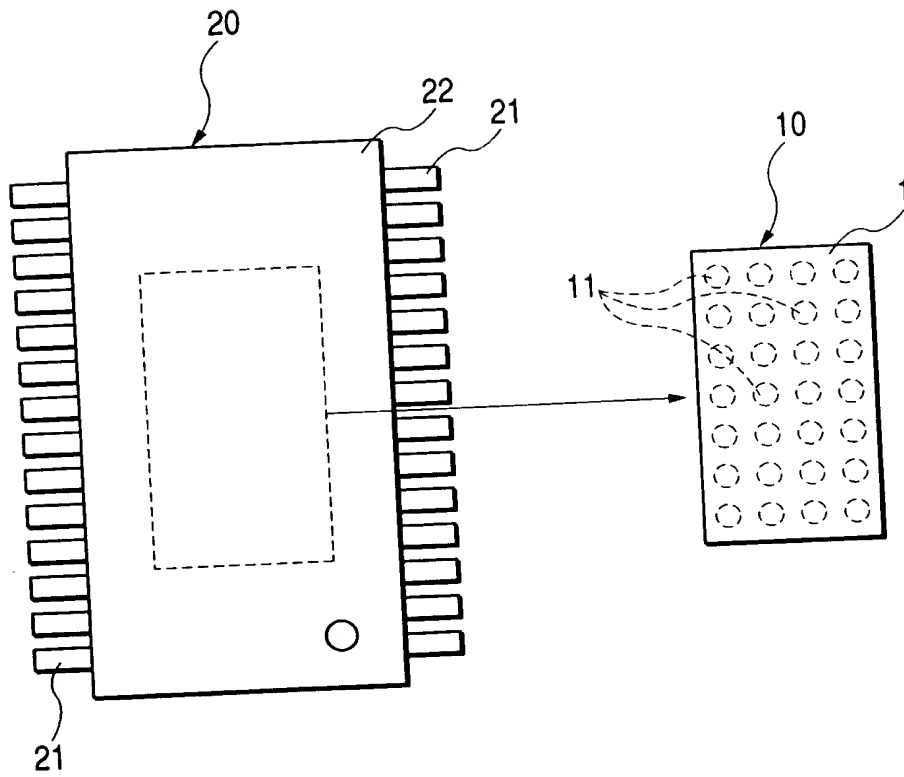


FIG. 5(a)

FIG. 5(b)



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graph TD; S1[WAFER PROCESS] --> S2[WPP - FORMING FIRST INSULATING LAYER]; S2 --> S3[WPP - FORMING RE - WIRING LAYER]; S3 --> S4[WPP - FORMING SECOND INSULATING LAYER]; S4 --> S5[WPP - FORMING UBM]; S5 --> S6[TEST OF WAFERS (W - TEST)]; S6 --> S7[TEST BY PROBE (P - TEST 1)]; S7 --> S8[LASER BLOWN FUSES]; S8 --> S9[TEST BY PROBE (P - TEST 2)]; S9 --> S10[MARKING ON BACK SURFACE OF THE WAFER]; S10 --> S11[FORMING OF BUMPS]; S11 --> S12[DICING]; S12 --> S13[AGING (BI)]; S13 --> S14[CHIP SORTING];
```

WAFER PROCESS S1

WPP - FORMING FIRST INSULATING LAYER S2

WPP - FORMING RE - WIRING LAYER S3

WPP - FORMING SECOND INSULATING LAYER S4

WPP - FORMING UBM S5

TEST OF WAFERS (W - TEST) S6

TEST BY PROBE (P - TEST 1) S7

LASER BLOWN FUSES S8

TEST BY PROBE (P - TEST 2) S9

MARKING ON BACK SURFACE OF THE WAFER S10

FORMING OF BUMPS S11

DICING S12

AGING (BI) S13

CHIP SORTING S14

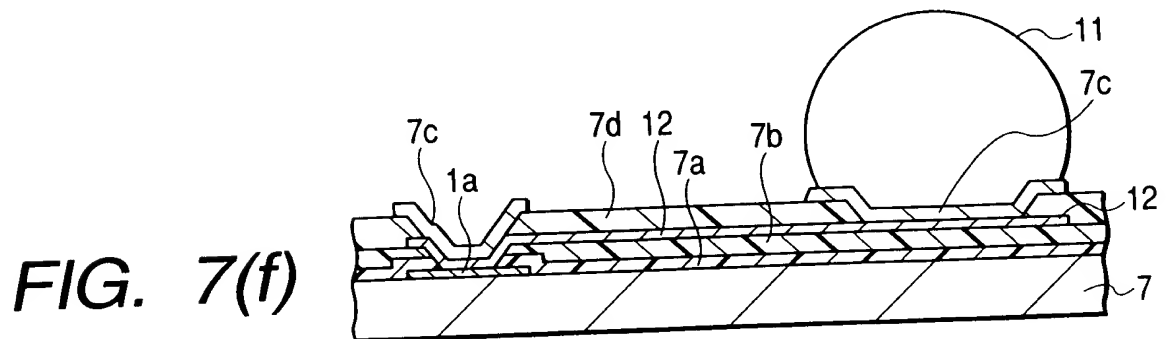
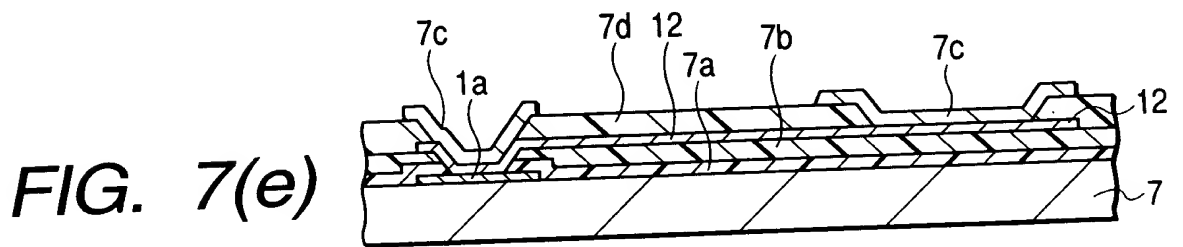
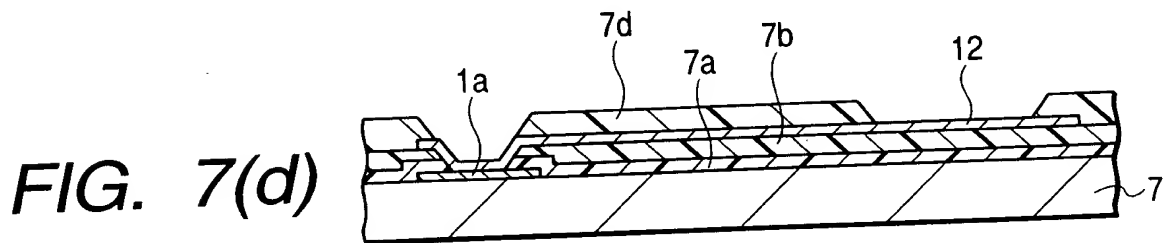
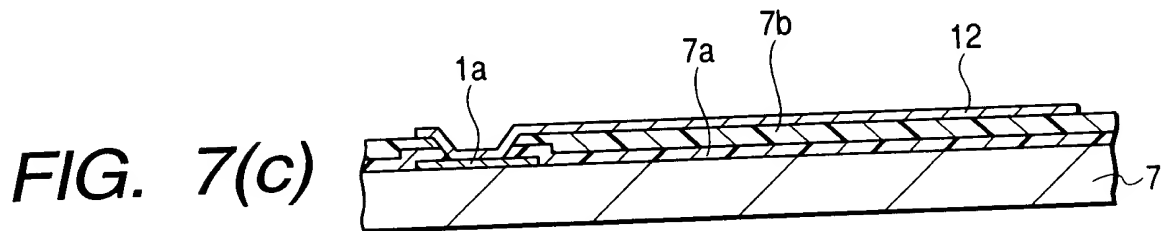
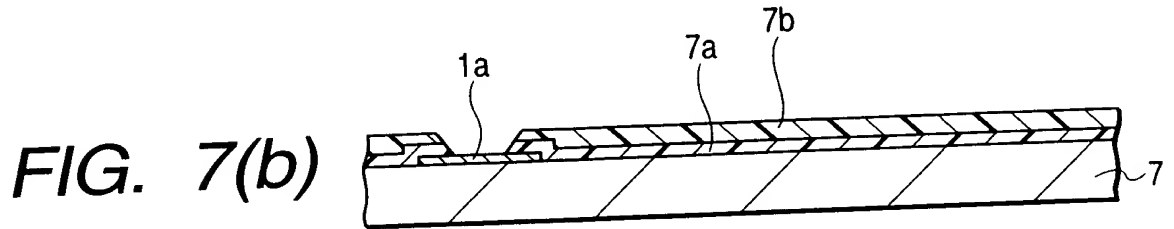
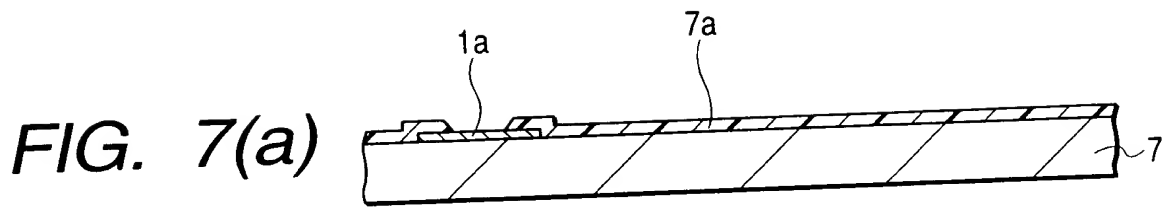


FIG. 8

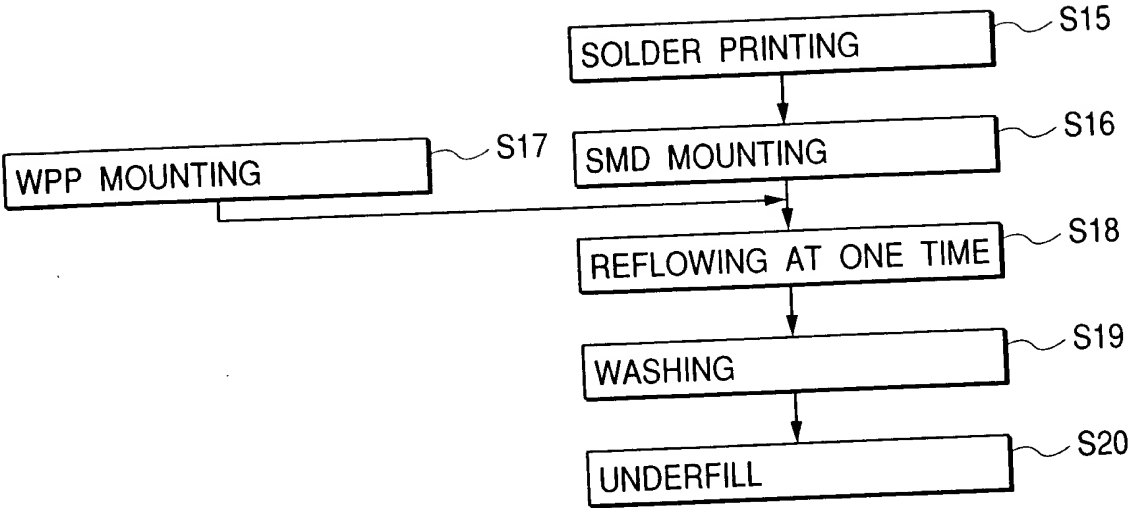
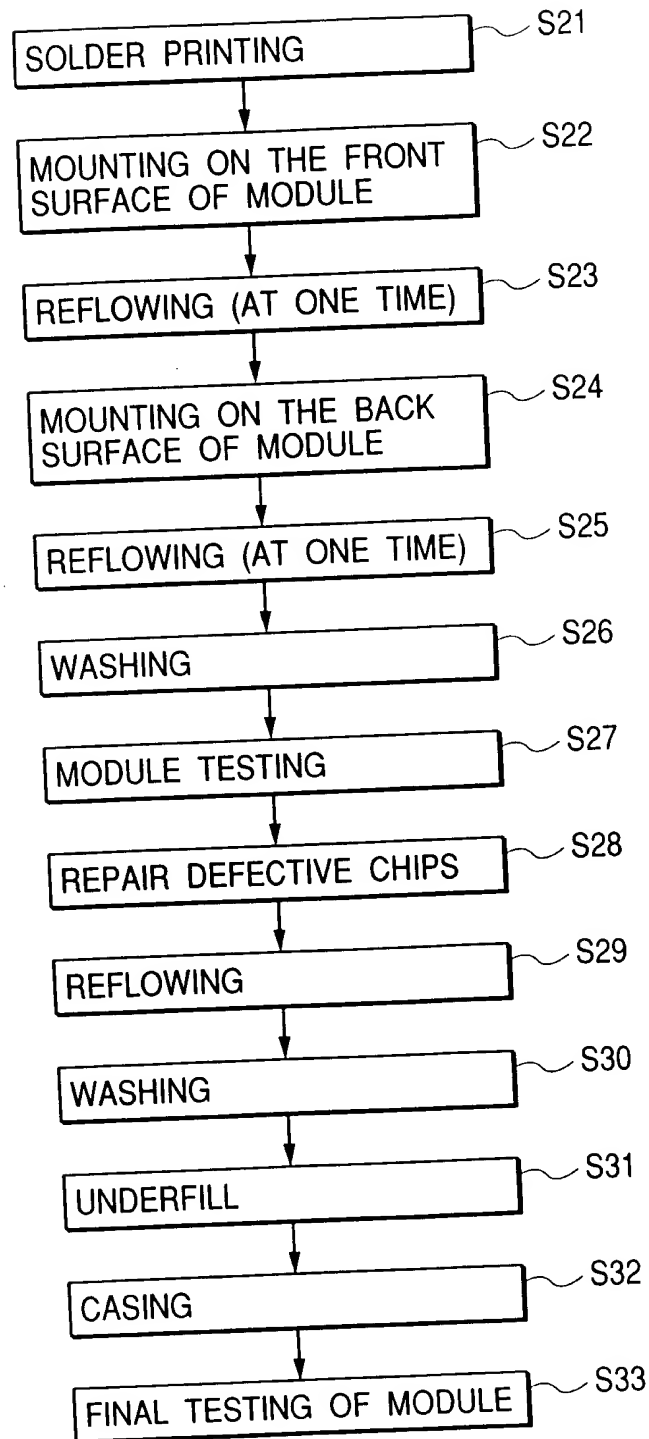


FIG. 9

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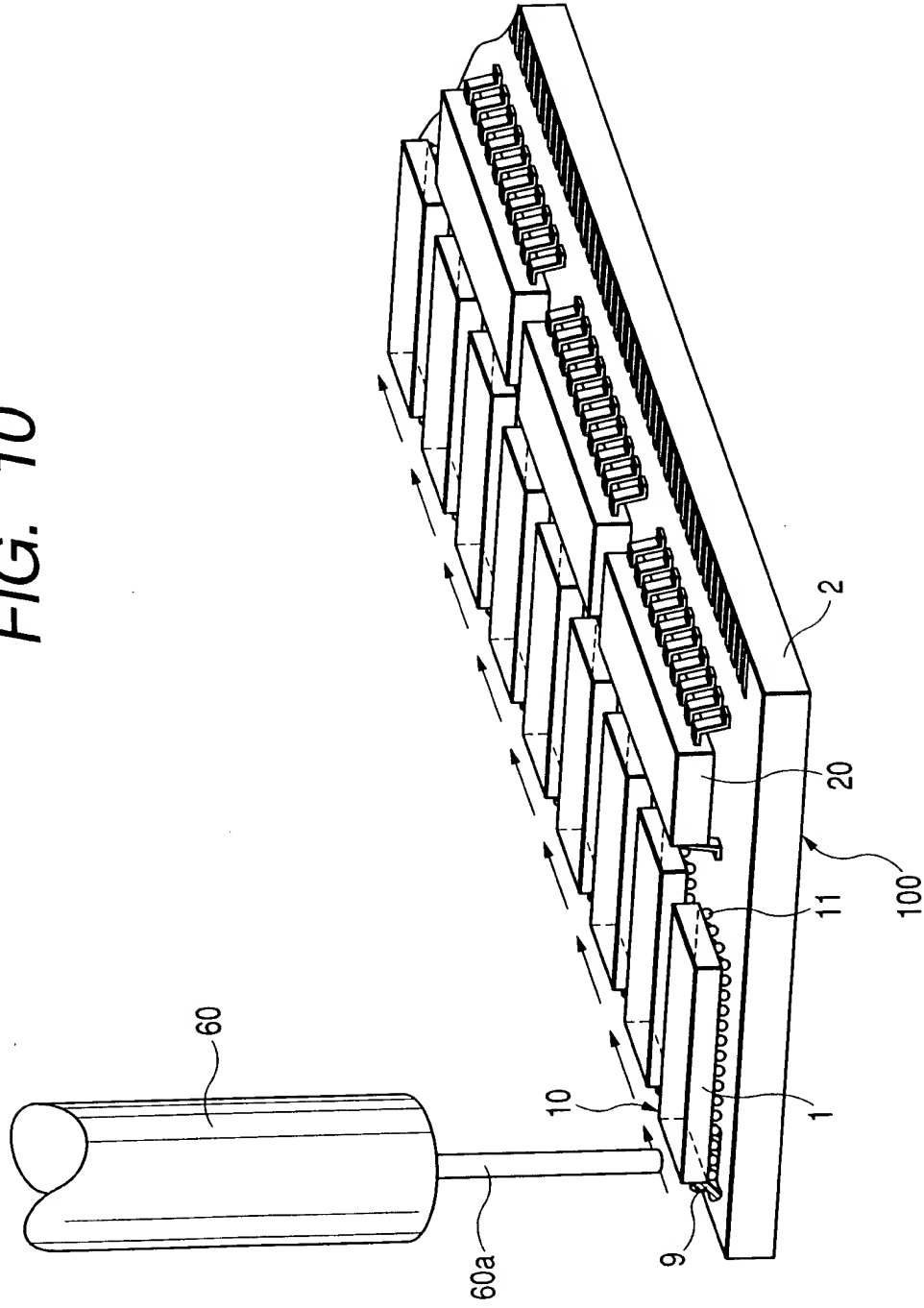


FIG. 10

FIG. 11(a) FIG. 11(c) FIG. 11(e) FIG. 11(g)

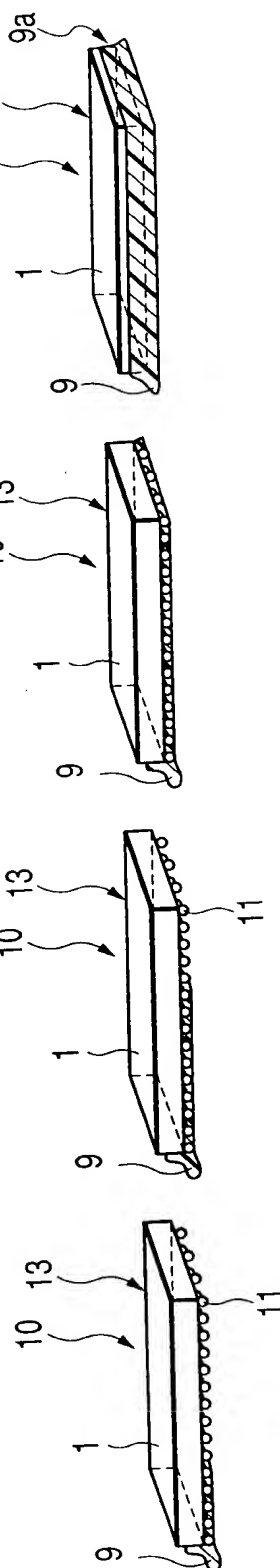
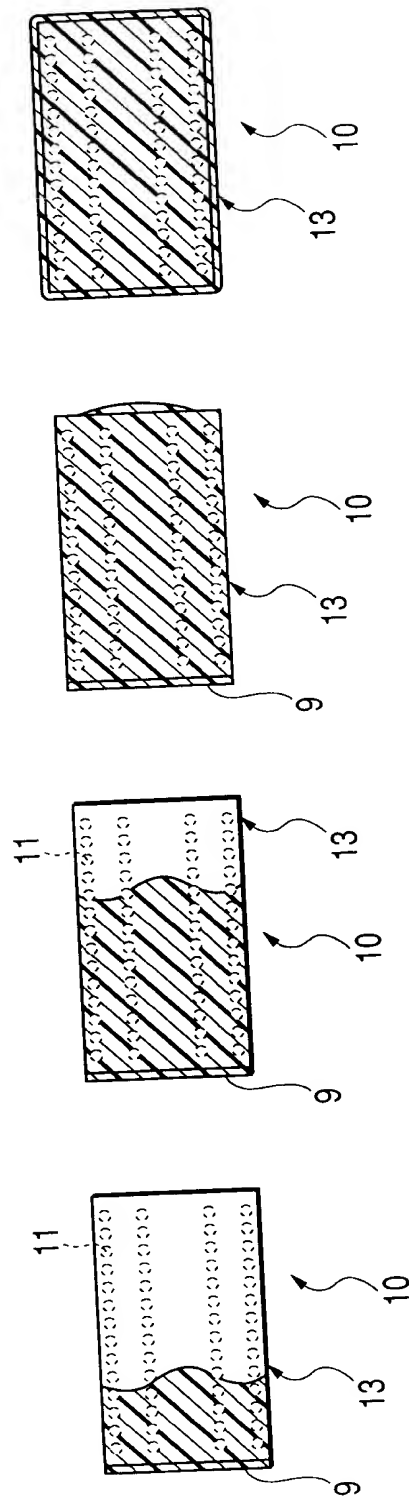


FIG. 11(b) FIG. 11(d) FIG. 11(f) FIG. 11(h)



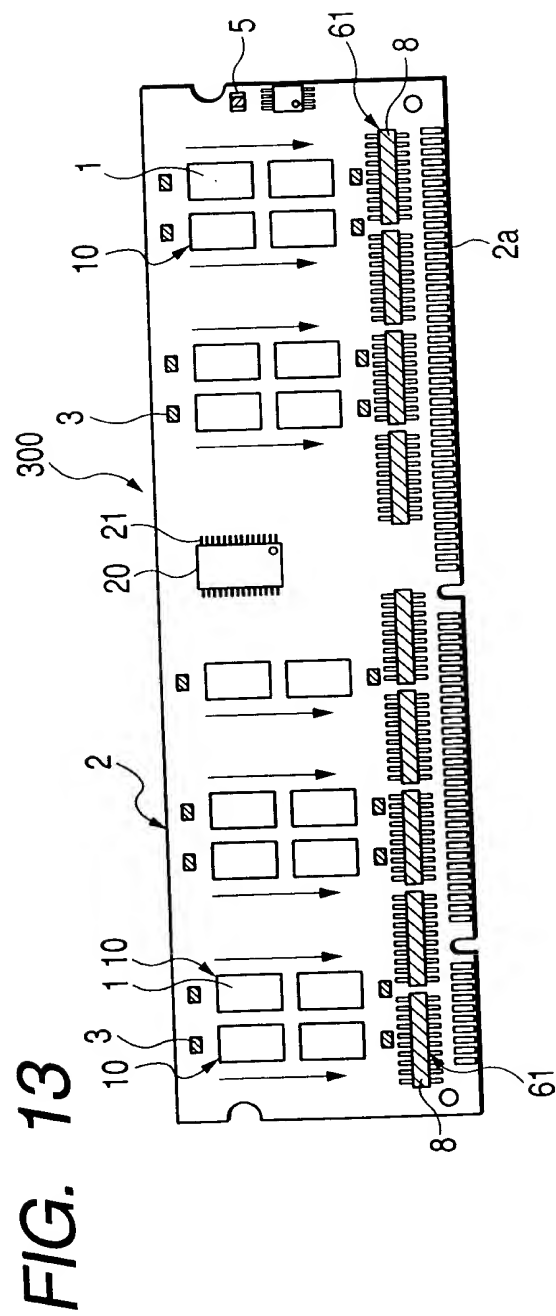
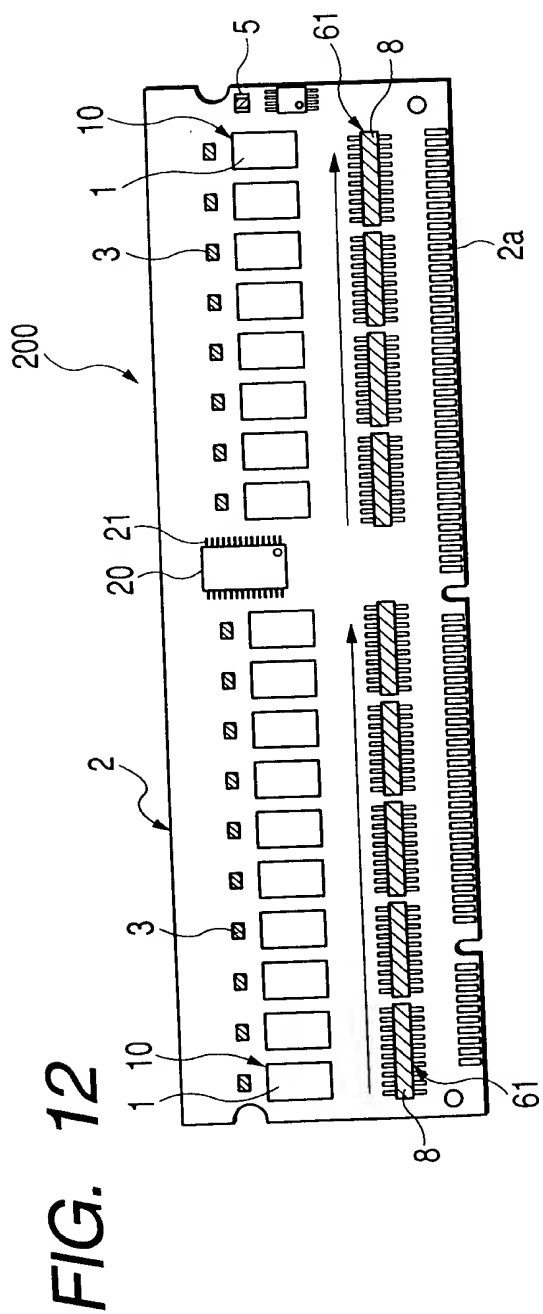


FIG. 14(a)

FIG. 14(c)

FIG. 14(e)

FIG. 14(g)

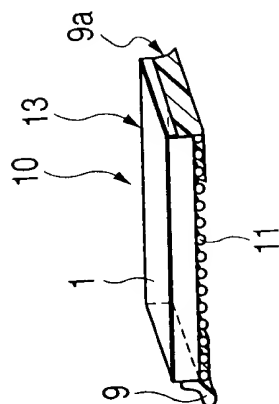
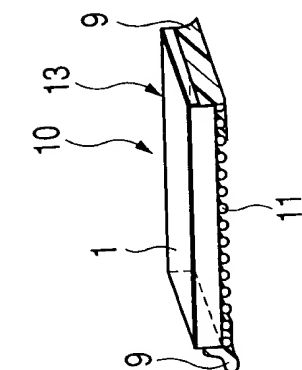
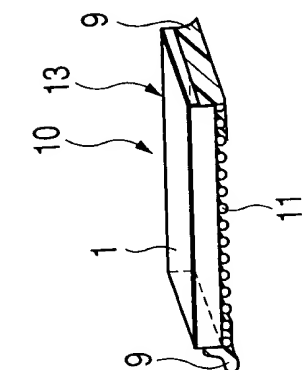
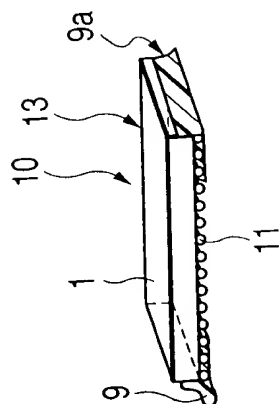


FIG. 14(b)

FIG. 14(d)

FIG. 14(f)

FIG. 14(h)

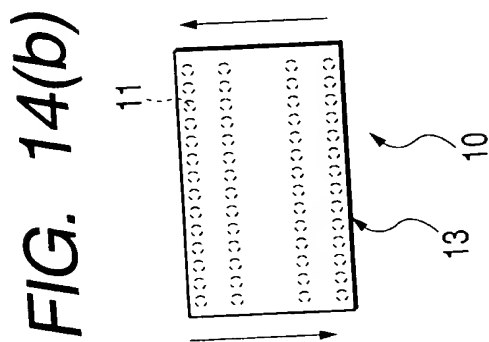
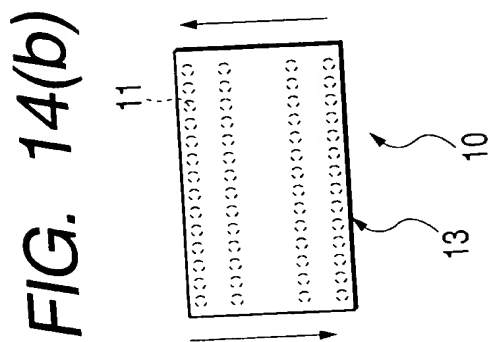
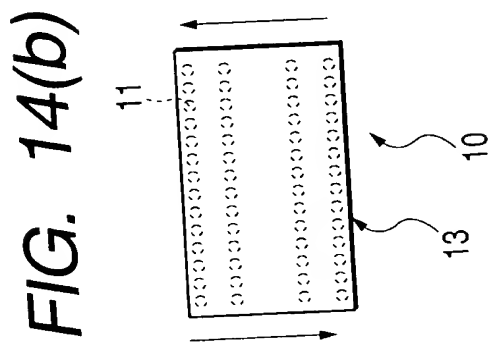
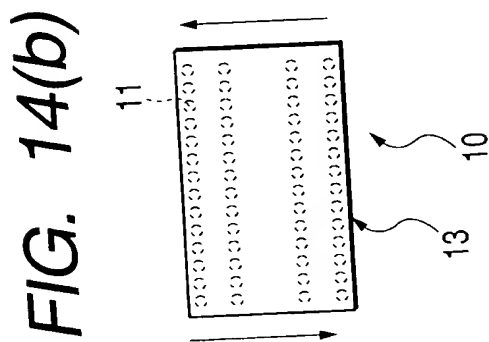


FIG. 15(a)

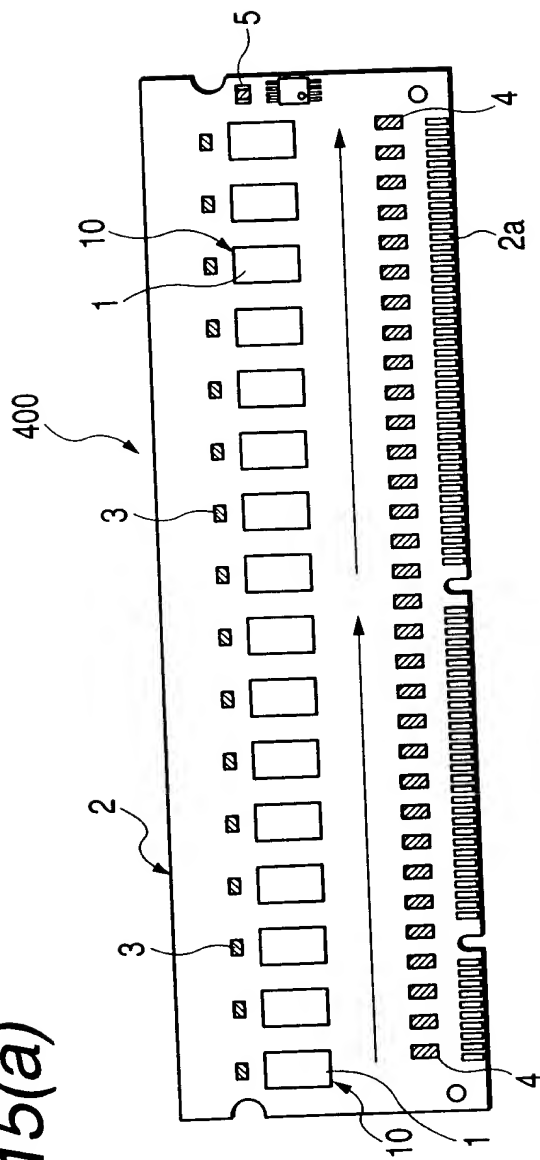


FIG. 15(b)

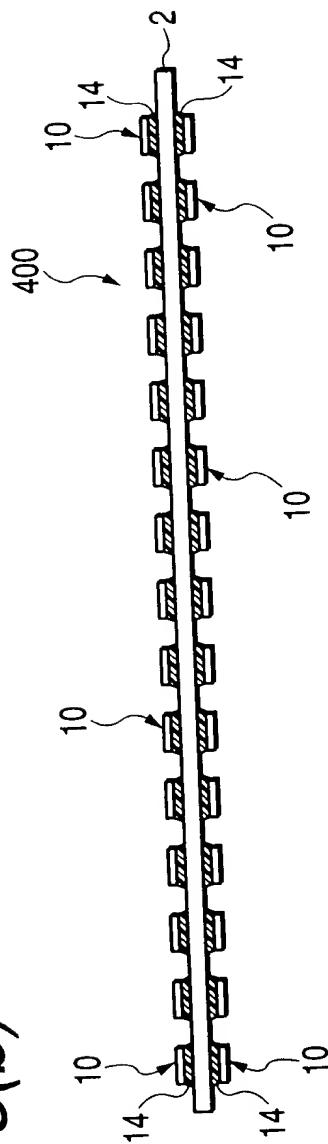


FIG. 16

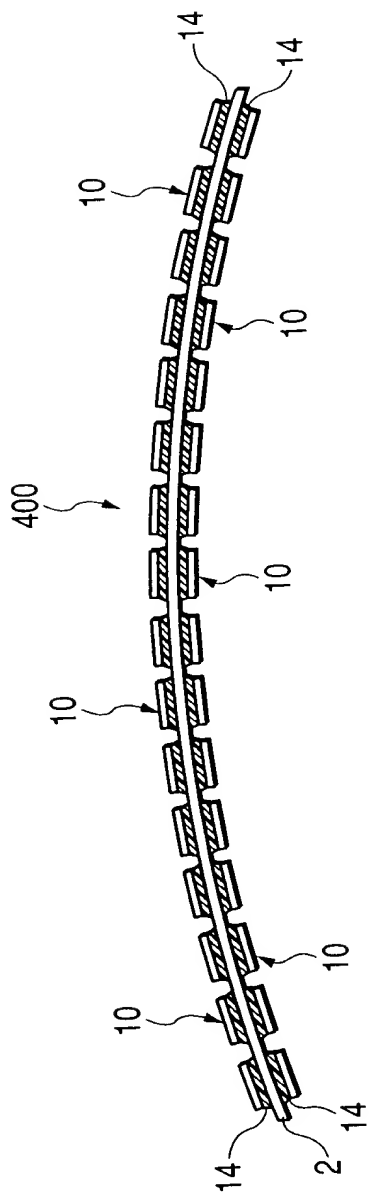
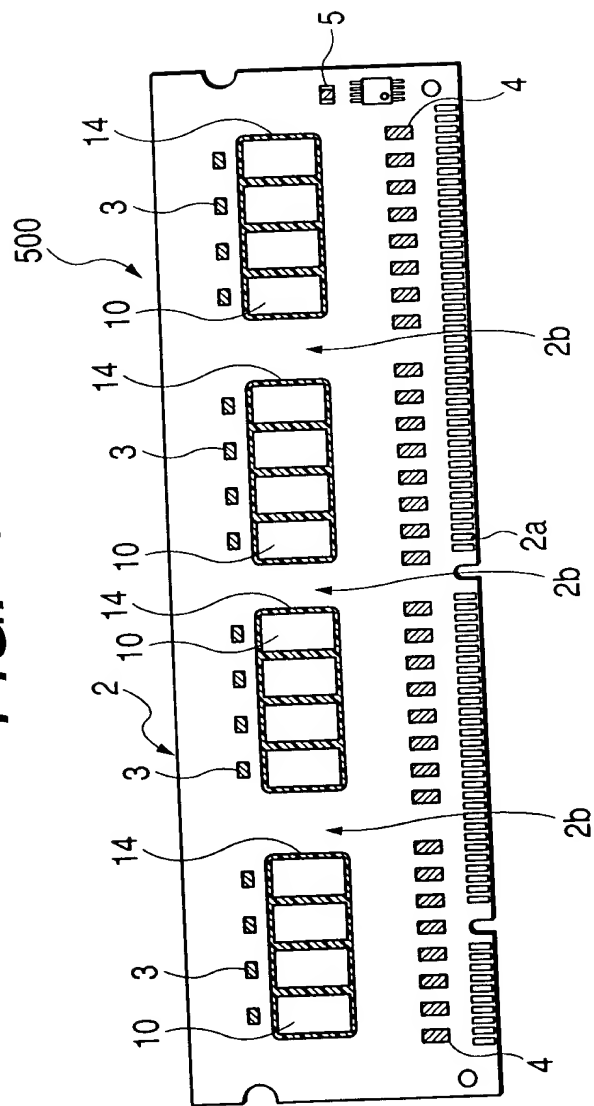


FIG. 17



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FIG. 18

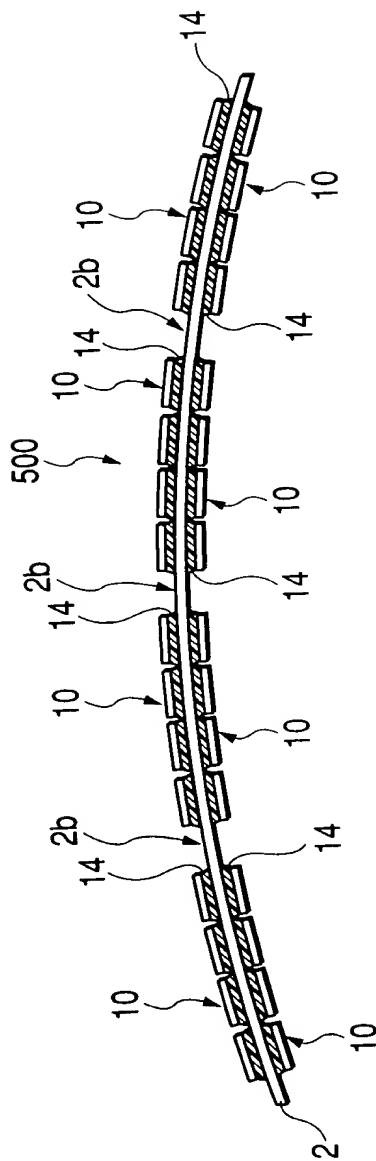


FIG. 19

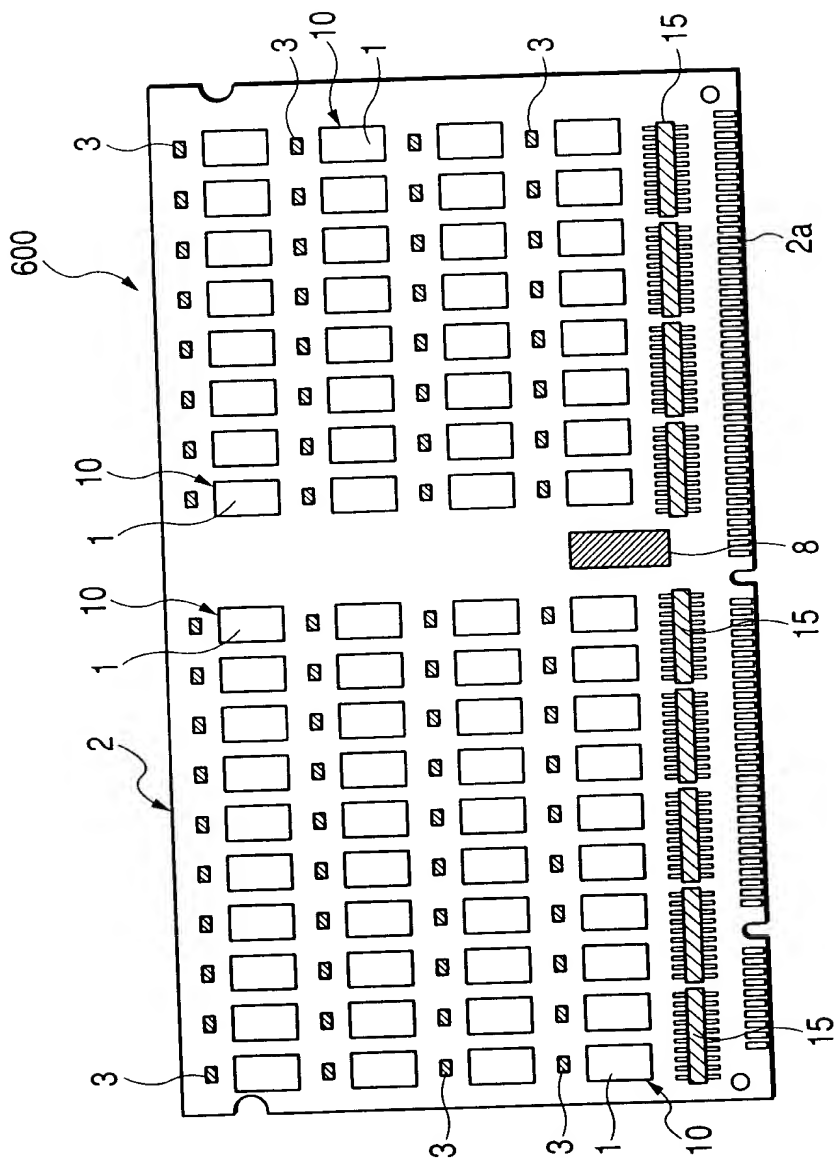


FIG. 20(a)

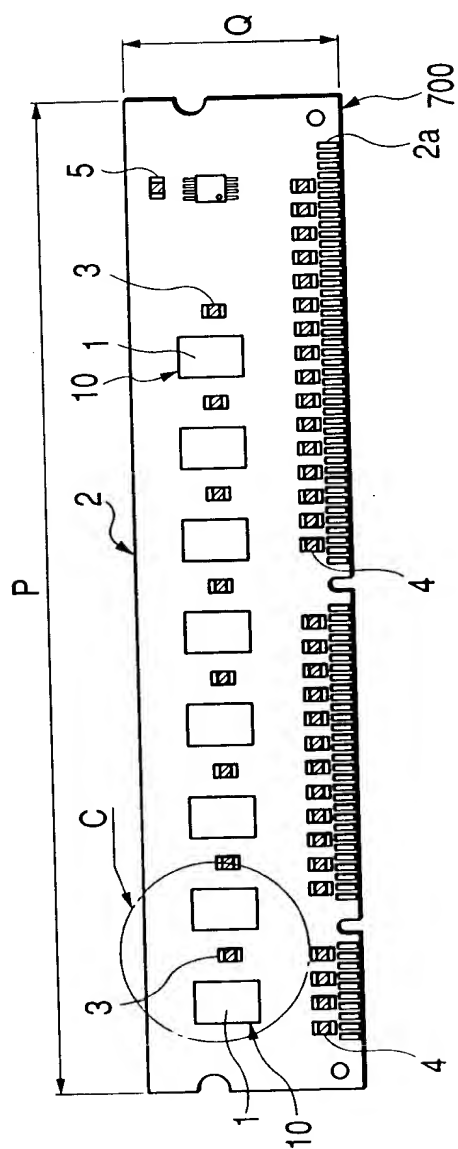


FIG. 20(b)

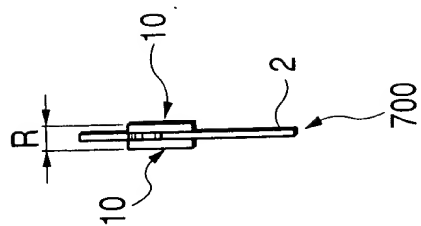


FIG. 21

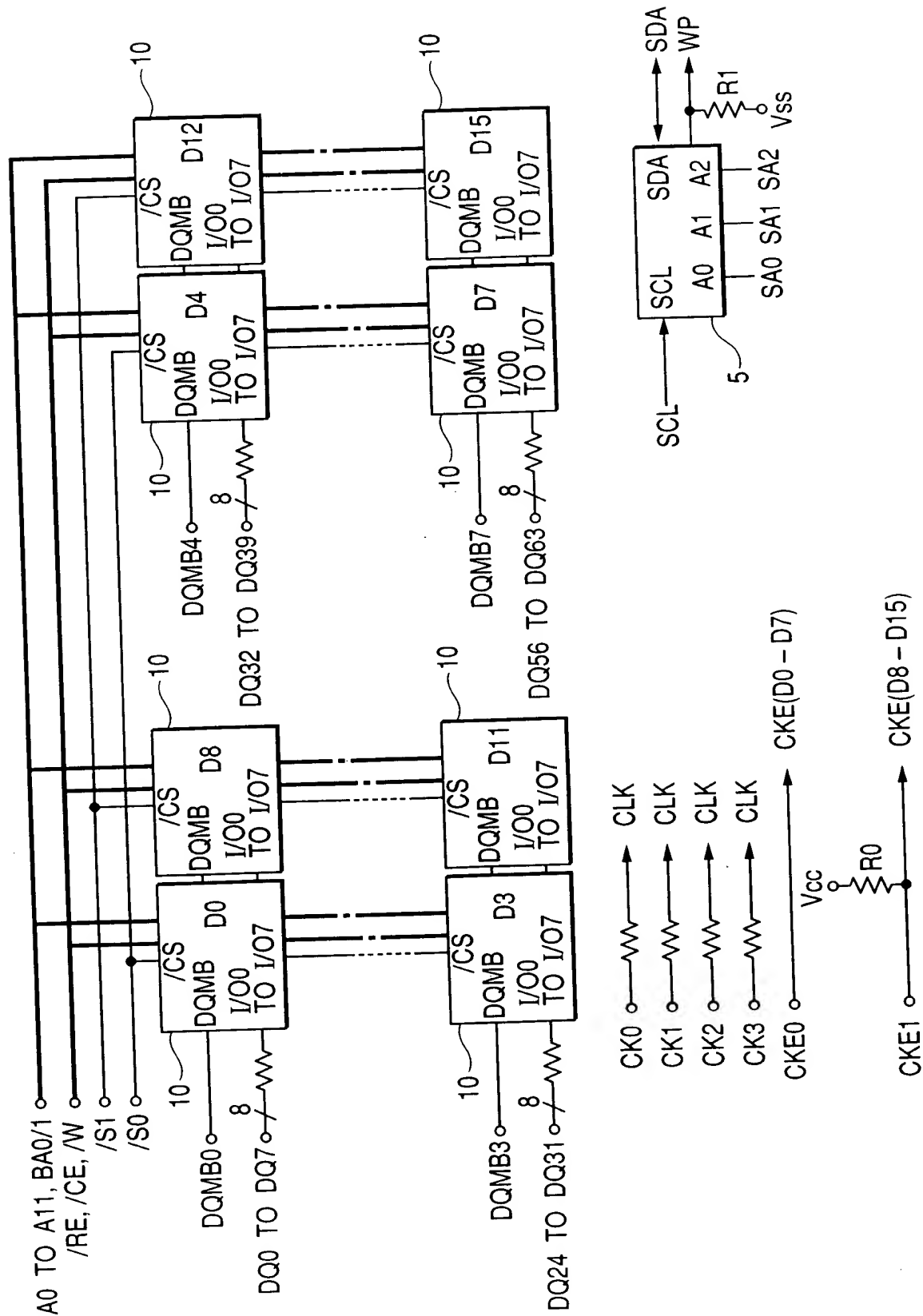


FIG. 24

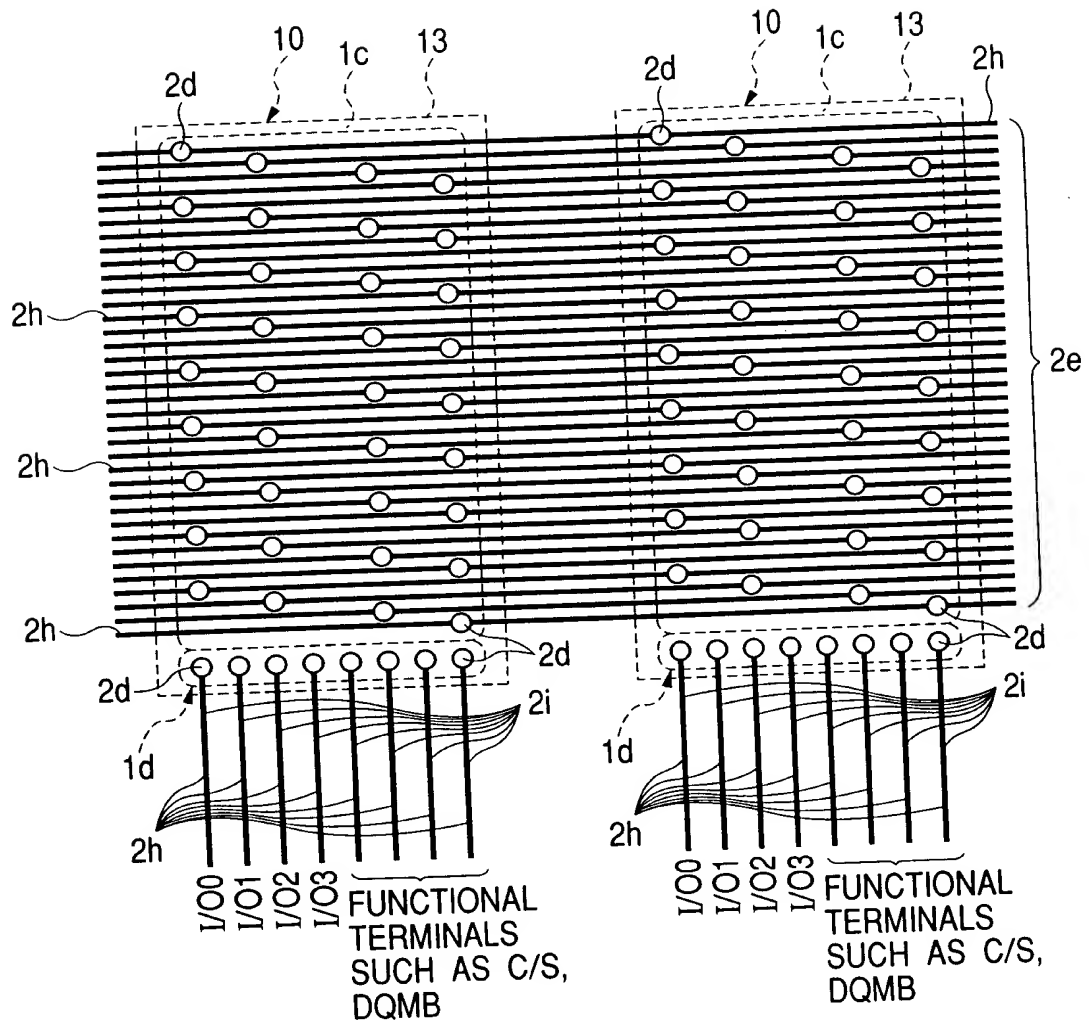


FIG. 25

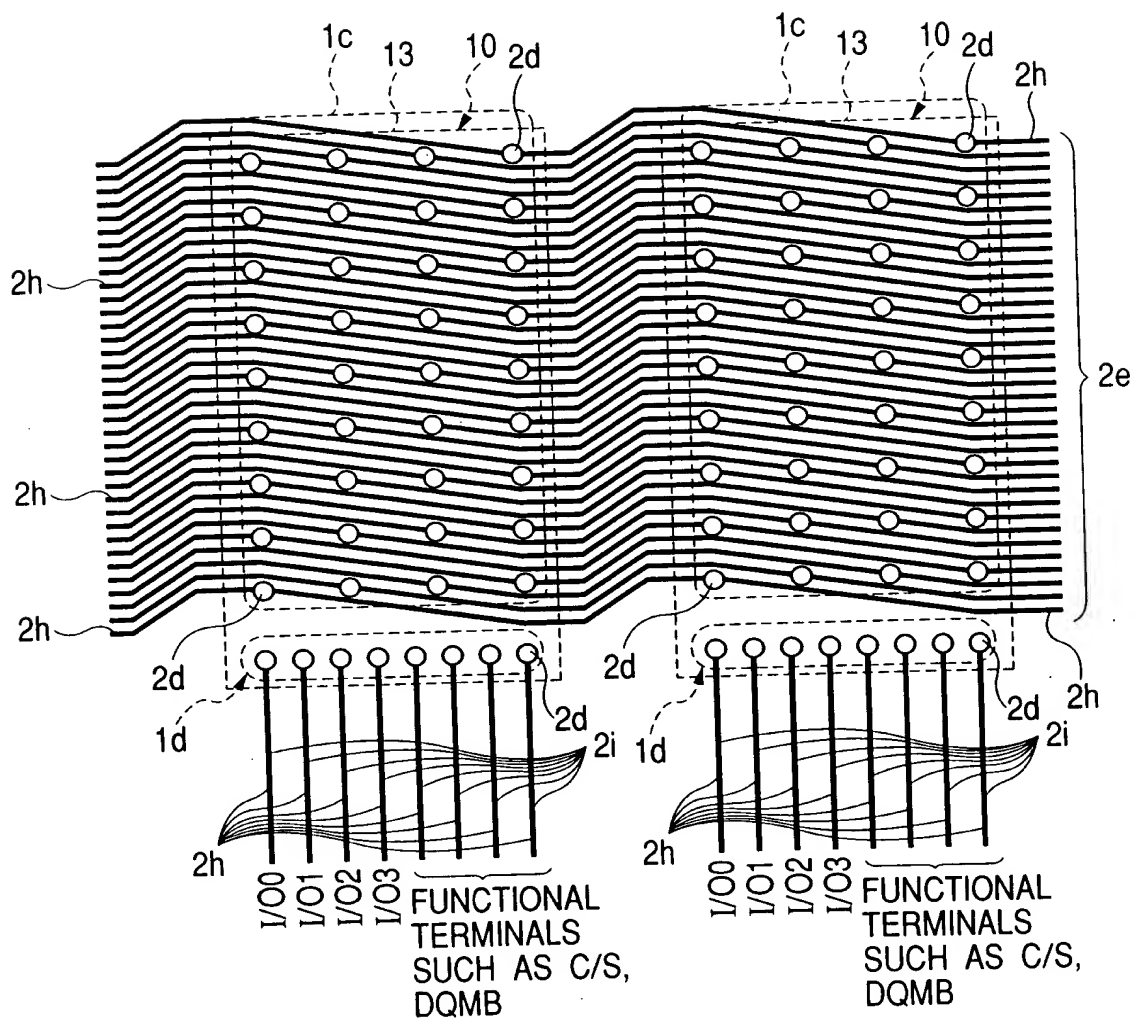


Figure 1 is a plan view of a semiconductor device. It shows two identical rectangular regions, each containing a grid of horizontal lines (10) and vertical lines (13) intersecting at points (1c). The regions are separated by a vertical gap (2h). The entire structure is labeled 2e. Below each region, there are four vertical lines (2i) labeled 1/00, 1/01, 1/02, and 1/03, which are functional terminals such as C/S, DQMB. The regions are also labeled 1d and 2d.

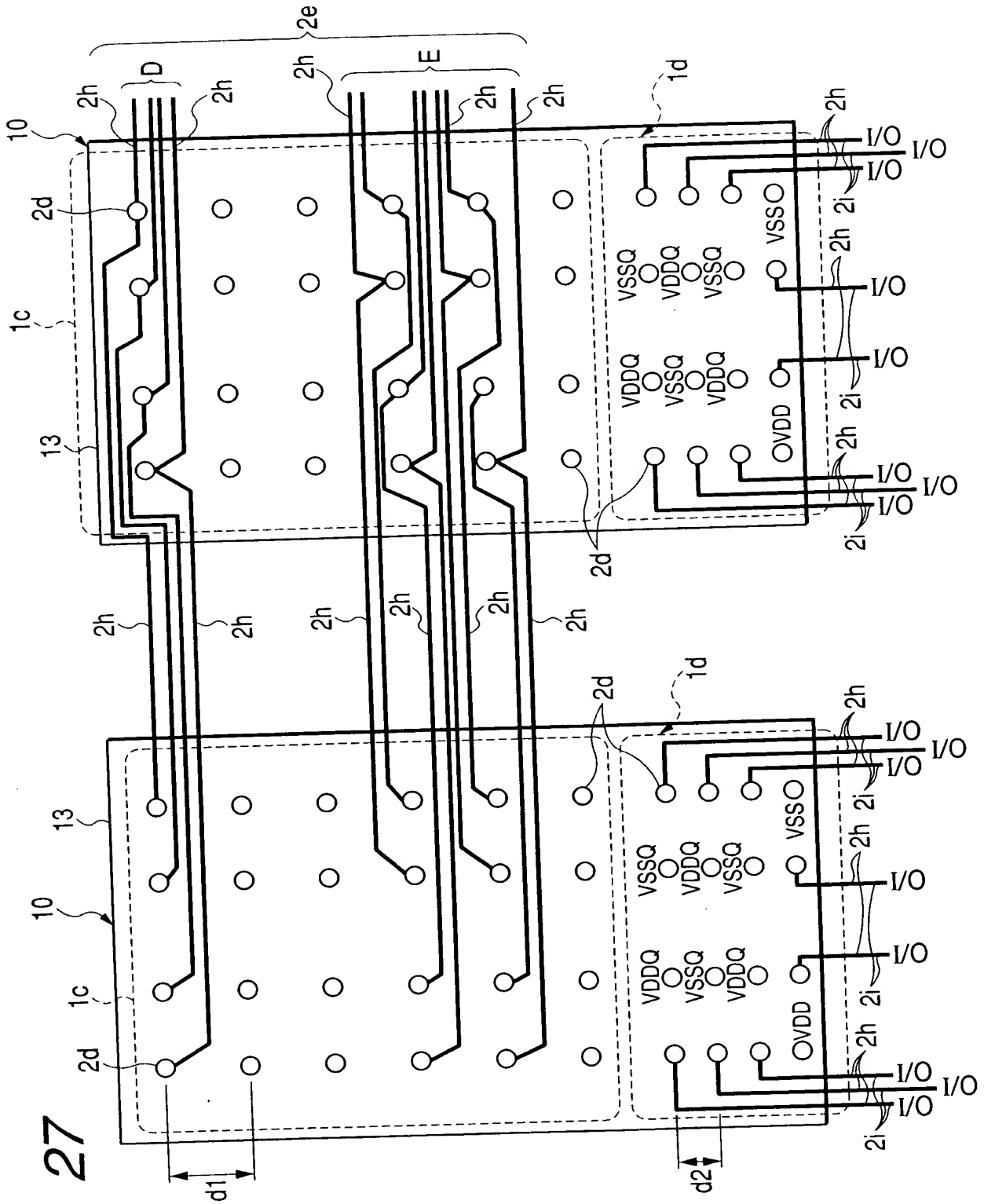


FIG. 27

FIG. 28(a)

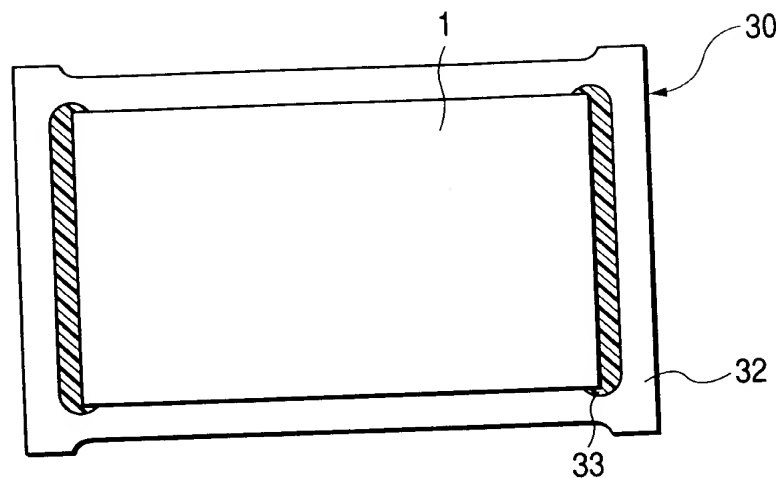


FIG. 28(b)

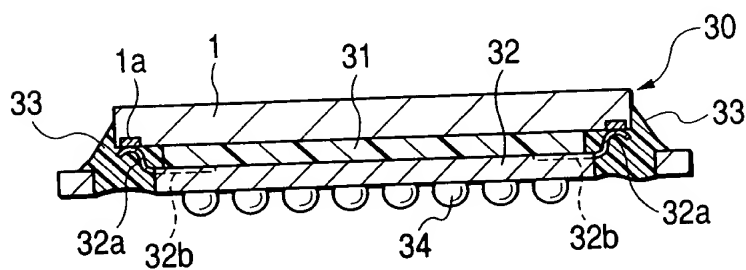
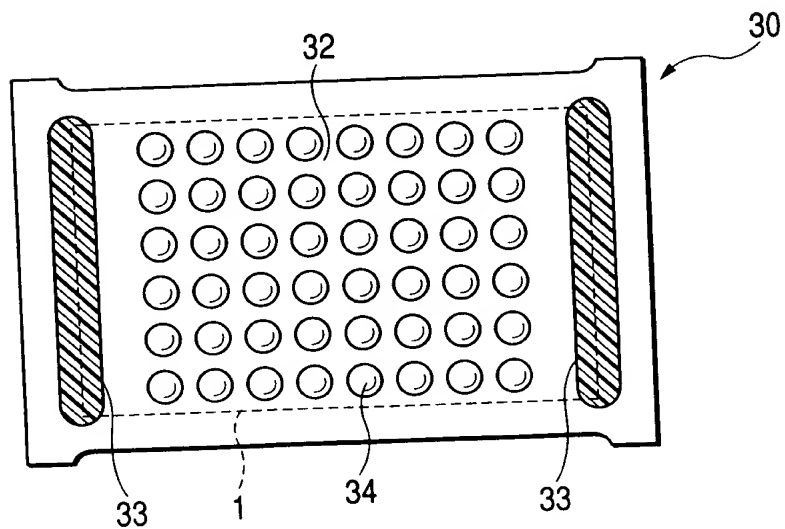


FIG. 28(c)



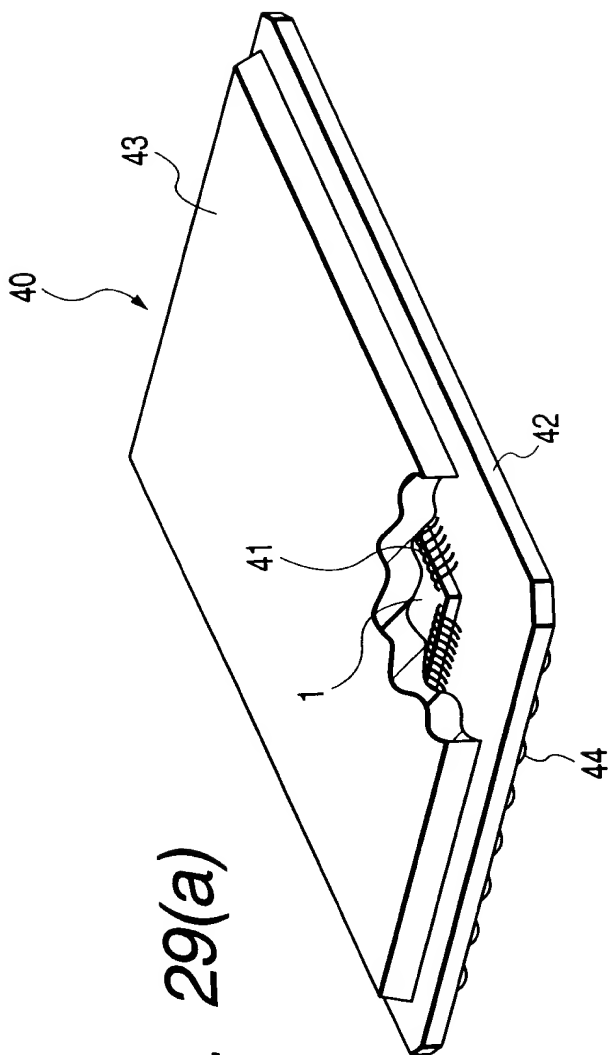


FIG. 29(a)

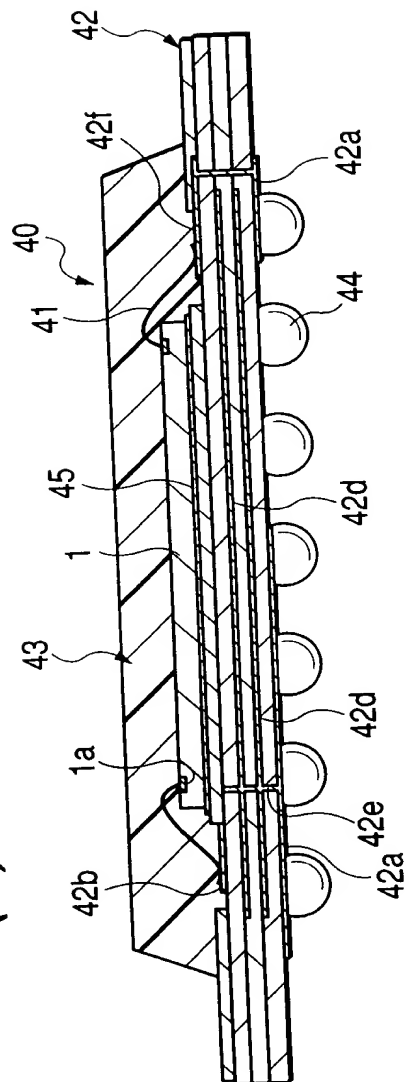


FIG. 29(b)

FIG. 30(a)

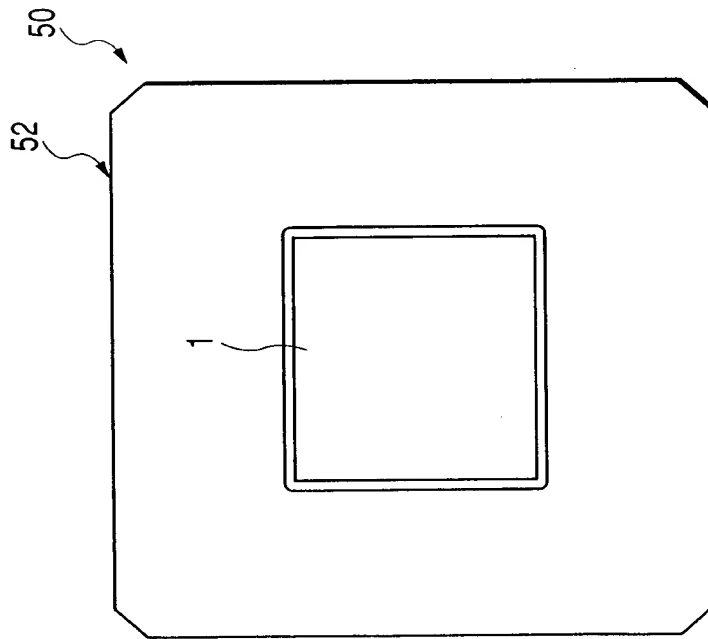


FIG. 30(c)

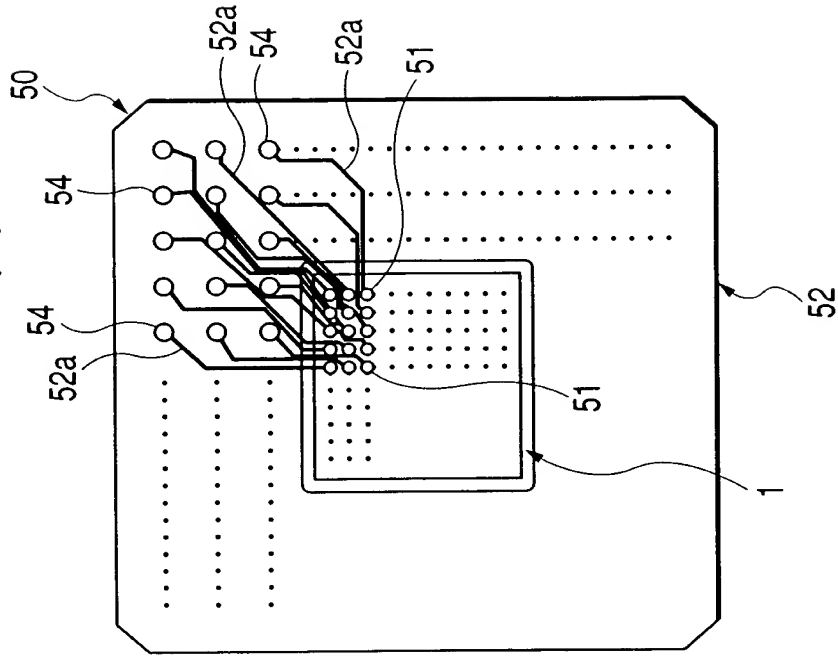


FIG. 30(b)

